IN THE SPECIFICATION

Please amend par. [0020] in the original specification (now represented as [0022] in the published specification), as follows:

[0020] FIG. 2 is a conceptual block diagram illustrating an example of a CDMA chip. The CDMA chip 106 includes a receiver front end 210, a searcher 220, a demodulator 230, and a decoder 240. The receiver front end 210 further includes multiplexers 212, 214, and 216, and receiver front end processing (e.g., RX_FRONT PROCESSING) 218. The receiver front end 210 accepts a digitized received signal 220 from an antenna (not shown) through an analog front end (not shown), and performs baseband filtering of the received digitized signal 220. Each of the multiplexers 212, 214, and 216 receives a corresponding selection signal that causes each multiplexer to selectively switch between passing the digitized received signal 220, at logic "0," or the test data pattern 382, at logic "1," (shown in FIG. 3 as test_pattern_i/q). The demodulator 230 performs initial CDMA signal processing on the filtered digitized signal such as, but not limited to, descrambling the signal with the various scrambling codes to identify the base station source of the transmission, and □ispreading the signal with the various OVSF codes to separate the traffic and control channels for each base station. Next, the decoder 240 may be used to provide additional signal processing functions such as, but not limited to, deinterleaving and decoding.